Minutes of Wednesday 2/5/03 RR BPM Meeting to discuss ECHOTEK DDC SIGNAL PROCESSING

Attending: C. Briegel, B. Choudhary, J. Crisp, P. Prieto, W. Schappert, D. Voy, B. Webber

Purpose of the meeting:
--- Hear results of Warren's signal processing simulation work
--- Identify and plan for what next needs to be done, especially plan for specific demonstation tests in the lab test setup
--- Work toward DDC/VME CPU data interface/definitions for each measurement type/mode
--- Identify responsibilities for contributions to this topic for Feb.17 RR BPM Technical Design Review

Warren described and presented results from his MatLab simulation of signal processing in the Graychip that included input signal attenuation and dispersion in tunnel-to-service building cabling. The model includes the data decimation characteristics of the Graychip. He showed a simulation that represented position measurement of one of four 2.5MHz bunches and showed that the "cross-talk" between bunches can be small. He also simulated the "cross-talk" between measured positions of bunched beam, hot beam, and cold beam as a function of beam intensities and positions for worst case conditions, i.e. maximum intensity in each interfering beam partition and minimum time separation between partitions. Results looked very promising. This work should provide strong evidence that the Echotek/Graychip board is suitable for the required measurements and should provide a jumpstart to demonstrating the board's suitability in the test lab. Warren will work to complete the write-up of his work to date.

Once again the question of the advisability of a "synchronous" digitizer clock came up. Discussions did not reach resolution except to establish a definition of what is mean by that term in this context. Definition: "Synchronous Clock" - a clock that is an integer multiple of the beam revolution frequency, Frev; equivalently, Fclock = (N/M) * Frf, where N/M = integer/588. Issue still unresolved, but not critical path. Warren will work toward understanding how/if synchronous clock really is beneficial. Bob is uncertain about range of Frev in RR over range of operating conditions.

Issue of handling signal skew on Echotek boards that have a common trigger to all eight channels was discussed. One solution since Warren's solutions use only a few non-zero coefficients on the "many-tapped" filters may be to shift non-zero coefficients along the taps so that outputs of filters are "in time". [Note: Since meeting Peter has spoken with EchoTek and they have agreed on specs for adding on-board channel independent trigger delays. We will plan to order boards with this feature.]

Duane observed that different Echotek set-up and measurement modes may imply different data streams and processing in the VME CPU; it's not so simple as one data point per trigger. This points out the urgency to define the scope and detail of set-ups and measurement modes. It plays into front-end hardware (available memory) and software requirements. The VME CPU boards are long lead-time items to procure.

Resolution of the specifics of each measurement mode probably depend on proving each mode in the test set-up. Peter and Charlie were assigned the task of specifying a list of first order test set-up activities.

There was some discussion of software requirements for operation of the test stand. It was ageeed that for now the plan is to begin with the software tools that now exist, including text file specification of DDC

filters, and evolve as the test stand is exercised.

Warren's write-up will be used as a reference for the Technical Design Review to be held ~Feb. 17th and Warren will be called upon to give a brief presentation on his work.

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